## WaferWave Technologies | Product Specification

# 100mm Prime Grade Silicon Wafer (CZ, P-Type, <100>)

**Product Overview:**

This high-purity Prime Grade substrate is engineered for advanced semiconductor fabrication, high-resolution lithography, and MEMS applications. Featuring an elite Total Thickness Variation (TTV) of <5 µm and ultra-low particle counts, this wafer ensures maximum yield for front-end-of-line (FEOL) processes.

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## 1. Physical & Crystallographic Properties

| Specification | Value |
|---|---|
| **Diameter** | 100 ± 0.3 mm |
| **Material** | Silicon (Si) |
| **Growth Method** | Czochralski (CZ) |
| **Grade** | Prime (Device Quality) |
| **Type / Dopant** | P-Type / Boron (P/B) |
| **Crystal Orientation** | <100> ± 0.5° |
| **Resistivity** | 1.0 – 5.0 Ω·cm |

## 2. Mechanical Specifications

| Specification | Value |
|---|---|
| **Thickness** | 525 ± 20 µm |

| | |
|---|---|
| **Total Thickness Variation (TTV)** | < 5 µm |
| **Bow** | < 30 µm |
| **Warp** | < 30 µm |
| **Orientation Features** | 2 SEMI-Standard Flats |
| **Primary Flat Location** | @ {110} ± 1° |
| **Primary Flat Length** | 32.5 ± 2.5 mm |
| **Secondary Flat Location** | 90° CW from Primary Flat |
| **Secondary Flat Length** | 18.0 ± 2.0 mm |

## 3. Surface & Purity Control

| Specification | Value |
|---|---|
| **Surface Finish (Front)** | Mirror Polished (SSP) |
| **Surface Finish (Back)** | Etched / Standard Finish |
| **Particle Count** | < 10 ea/wf (@ ≥ 0.3 µm) |
| **Laser Mark** | None |

## 4. Packaging & Documentation

| Specification | Value |
|---|---|
| **Packaging** | 25-Slot Polypropylene Cassette (Standard Wafer Jar) |
| **Sealing** | Double-bagged, Vacuum-sealed, ESD-protected |

| | |
|---|---|
| **Compliance** | Full Certificate of Analysis (COA) / Conformance (COC) included |

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